

ABSTRACT

This invention relates to an MRAM array architecture which incorporates certain advantages from both cross-point and 1T-1MTJ architectures during reading operations. The fast read-time and higher signal to noise ratio of the 1T-1MTJ architecture and the higher packing density of the cross-point architecture are both exploited by using a single access transistor to control the reading of multiple stacked columns of MRAM cells each column being provided in a respective stacked memory layer.